WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device, comprising:

depositing an oxide layer on a semiconductor substrate;

depositing a nitride layer on the oxide layer;

forming an opening in the oxide layer and the nitride layer exposing a field region of the semiconductor substrate;

forming a trench in the semiconductor substrate in the exposed region in the opening;

removing the oxide layer and the nitride layer;

forming a silicon epitaxial layer having a predetermined thickness pattern on the semiconductor substrate and the trench;

depositing an insulating layer in the trench; and

planarizing the insulating layer.

2. The method for manufacturing a semiconductor device as claimed in claim 1, wherein the silicon epitaxial layer is formed in such a manner that a portion thereof at a sidewall of the trench has a thickness greater than a thickness of the silicon expitaxial layer at a bottom portion of the trench.

3. The method for manufacturing a semiconductor device as claimed in claim 1, wherein the silicon epitaxial layer has an increased thickness is at an upper edge portion of the trench.

4. The method for manufacturing a semiconductor device as claimed in claim 1, wherein the insulating layer is formed by one of an O3-Tetra-Ortho-Silicate-Glass Atmospheric Pressure CVD process, Plasma Enhanced CVD process, and High Density Plasma CVD process.

5. The method for manufacturing a semiconductor device as claimed in claim 1, wherein the nitride layer is etched with a phosphoric acid solution.

6. The method for manufacturing a semiconductor device as claimed in claim 1, wherein the oxide layer is etched with a HF solution.

7. The method for manufacturing a semiconductor device as claimed in claim 1, wherein the insulating layer is planarized by Chemical Mechanical Polishing.

8. The method for manufacturing a semiconductor device as claimed in claim 7, wherein the insulating layer exists in only the trench after being planarized.

9. The method for manufacturing a semiconductor device as claimed in claim 2, wherein the silicon epitaxial layer has a thickness at an upper edge portion of the trench that is greater than the thickness of the silicon epitaxial layer at the sidewall of the trench.

10. The method according to claim 9, wherein the silicon epitaxial layer has a curved cross section at the upper edge of the trench.

11. The method according to claim 3, wherein the silicon epitaxial layer has a curved cross section at the upper edge of the trench.